Design Advisory: XS1-U and XS1-A series ADC noise

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Issue description

Significant noise can be observed on ADC readings on the U and A series devices. For a 0 to 3.3 volt signal, this issue can introduce errors of ±50mV.

The severity of the issue is application dependent. For highly sensitive applications requiring maximum sample frequency, the issue can be critical. For applications where sensitivity is not crucial, and or oversampling and averaging techniques can be used, the severity can be regarded as normal, with workarounds available.

The issue is illustrated in the graph below, which shows the results of a stress test using the following approach:

- An input voltage is applied, of between 1.522V and 1.600V.
- A set of 1000000 samples is taken.
- The ADC is measured
- The input voltage is incremented by 1 mV and the steps above are repeated

Throughout the test a 1MHz signal is driven out of 56 output ports to artificially create noise.
The following graph shows the results of this test, mapped onto a contour chart.

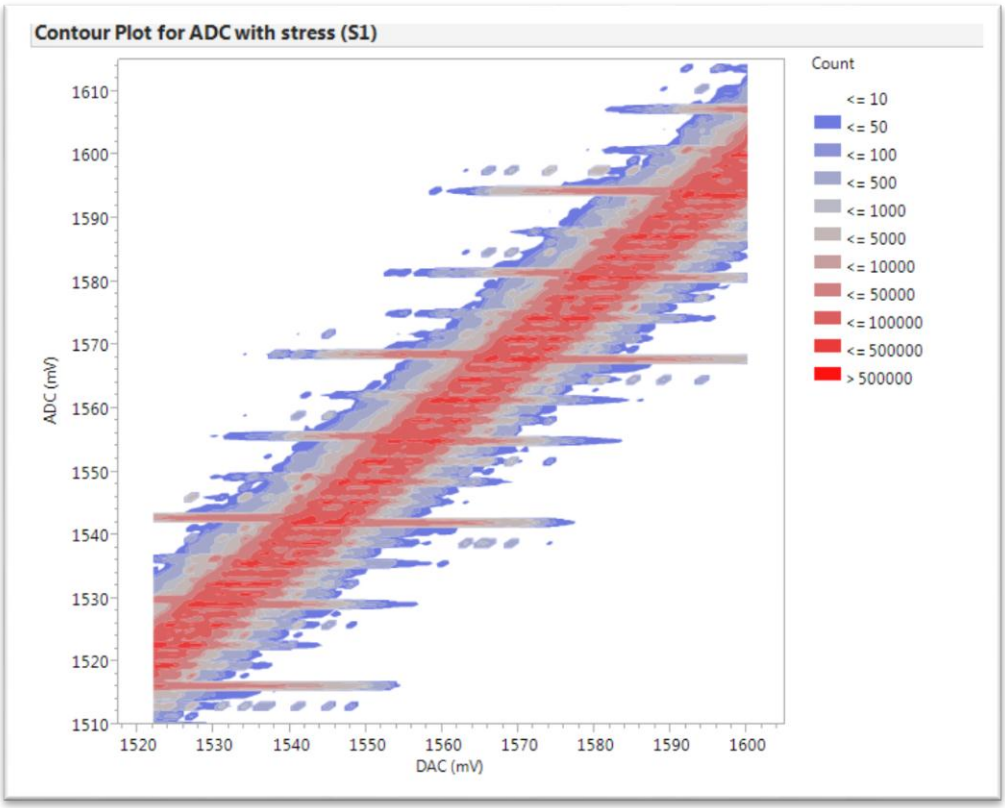


Figure 1: XS1-U6A-64 and XS1-U8A-64 under stress

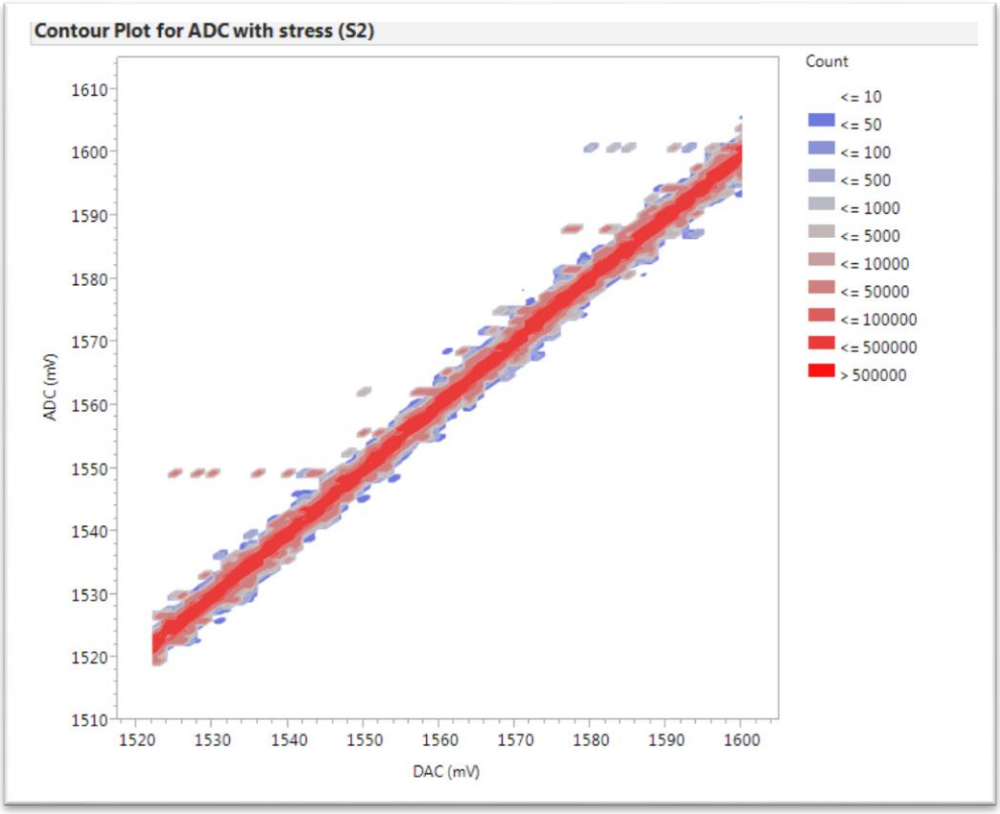


Figure 2: XS1-U8A-128, XS1-U10A-128, XS1-U12A-128 and XS1-U16A under stress

Affected devices and firmwares

The following devices are affected:

- XS1-U6A-64-FB96-C4
- XS1-U6A-64-FB96-I4
- XS1-U6A-64-FB96-C5
- XS1-U6A-64-FB96-I5
- XS1-U8A-64-FB96-C4
- XS1-U8A-64-FB96-I4
- XS1-U8A-64-FB96-C5
- XS1-U8A-64-FB96-I5

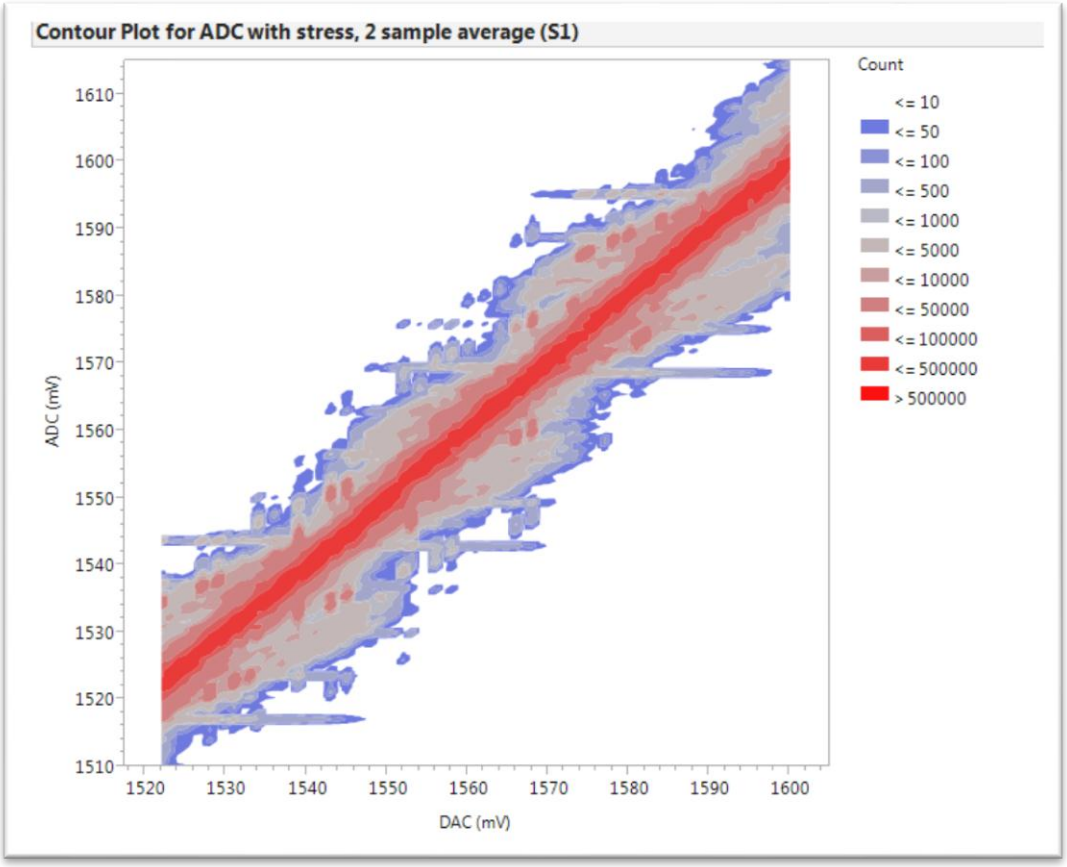
- XS1-A6A-64-FB96-C4
- XS1-A6A-64-FB96-I4
- XS1-A6A-64-FB96-C5
- XS1-A6A-64-FB96-I5
- XS1-A8A-64-FB96-C4
- XS1-A8A-64-FB96-I4
- XS1-A8A-64-FB96-C5
- XS1-A8A-64-FB96-I5

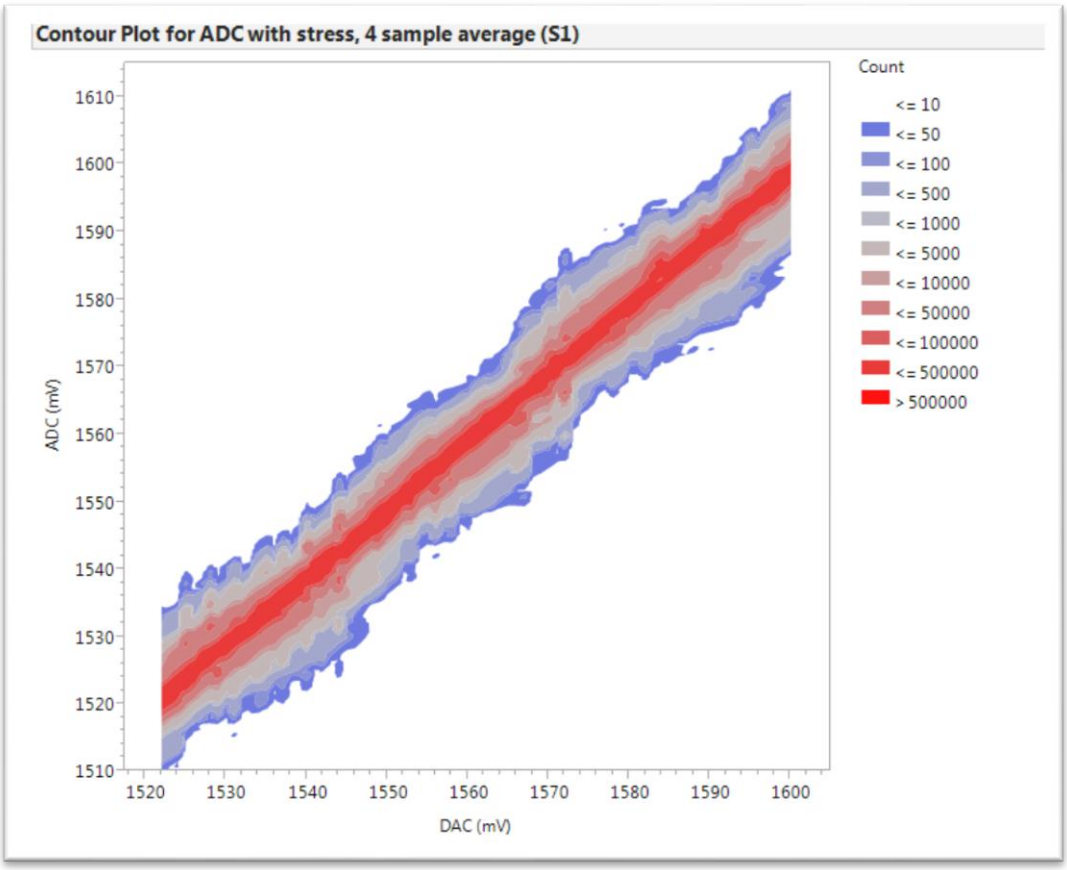
- XS1-U8A-128-FB217-C10
- XS1-U8A-128-FB217-I10
- XS1-U8A-128-FB217-I14
- XS1-U8A-128-FB217-C14
- XS1-U10A-128-FB217-C10
- XS1-U10A-128-FB217-I10
- XS1-U12A-128-FB217-C10
- XS1-U12A-128-FB217-I10
- XS1-U16A-128-FB217-C10
- XS1-U16A-128-FB217-I10

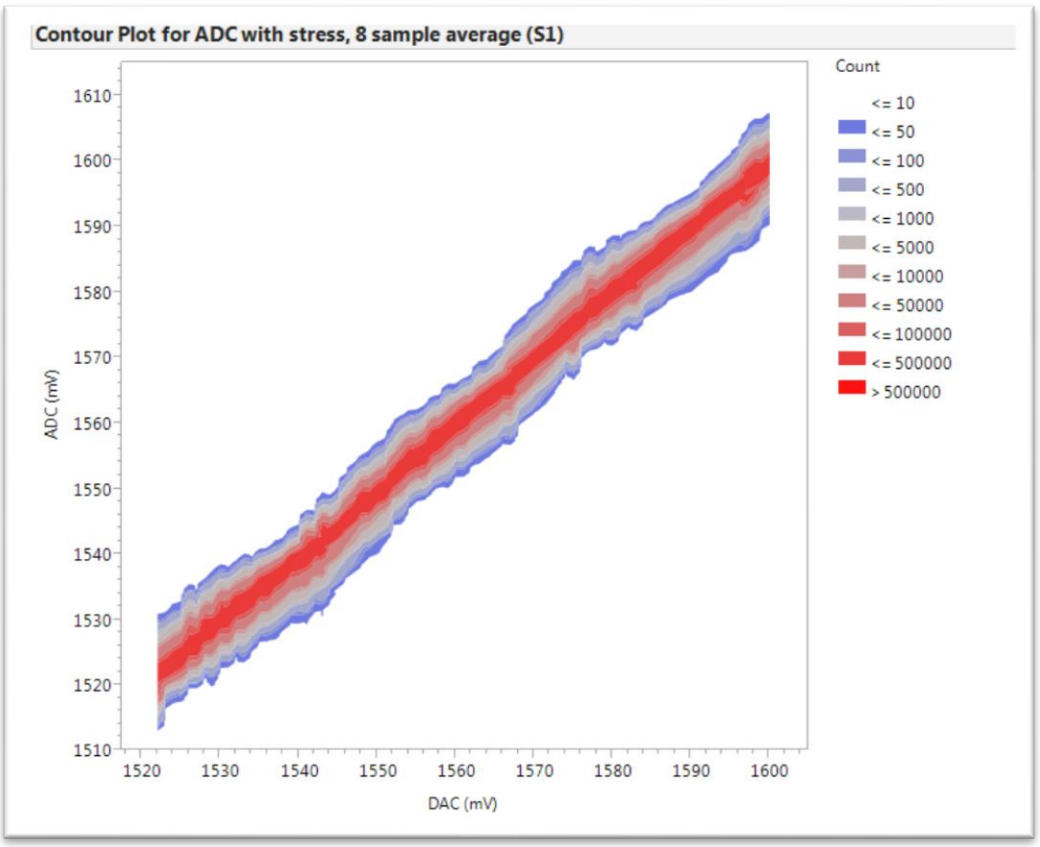
- XS1-A8A-128-FB217-C10
- XS1-A8A-128-FB217-I10
- XS1-A8A-128-FB217-I14
- XS1-A8A-128-FB217-C14
- XS1-A10A-128-FB217-C10
- XS1-A10A-128-FB217-I10
- XS1-A12A-128-FB217-C10
- XS1-A12A-128-FB217-I10
- XS1-A16A-128-FB217-C10
- XS1-A16A-128-FB217-I10

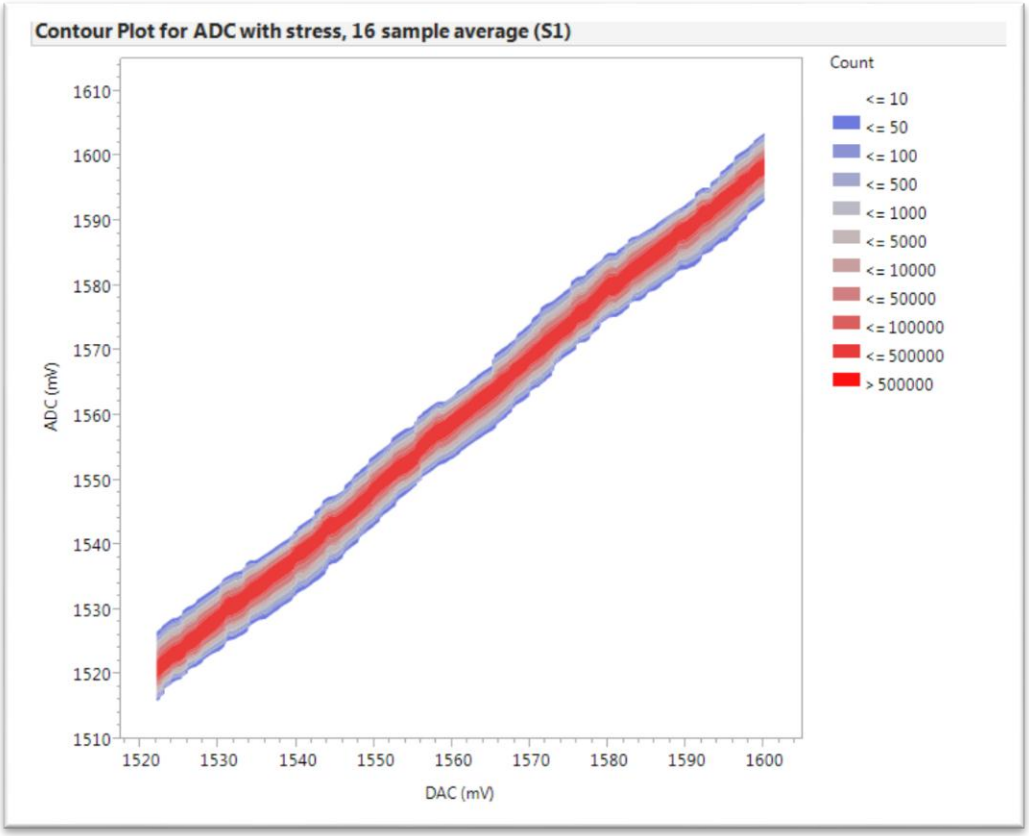
Recommended actions

Noise can be reduced by taking an average over several readings. The graphs below show the effect of averaging on the XS1-U8A-64-FB96-C5 when applied to n-million samples per input voltage step, where 'n' is the number of averaged samples.




Contour Plot for ADC with stress, 4 sample average (S1)
Count
<= 10
<= 50
<= 100
<= 500
<= 1000
<= 5000
<= 10000
<= 50000
<= 100000
<= 500000
> 500000
ADC (mV)
1610
1600
1590
1580
1570
1560
1550
1540
1530
1520
1510
1520
1530
1540
1550
1560
1570
1580
1590
1600
DAC (mV)


Contour Plot for ADC with stress, 8 sample average (S1)
Count
<= 10
<= 50
<= 100
<= 500
<= 1000
<= 5000
<= 10000
<= 50000
<= 100000
<= 500000
> 500000
ADC (mV)
1610
1600
1590
1580
1570
1560
1550
1540
1530
1520
1510
1520
1530
1540
1550
1560
1570
1580
1590
1600
DAC (mV)


Contour Plot for ADC with stress, 16 sample average (S1)
Count
<= 10
<= 50
<= 100
<= 500
<= 1000
<= 5000
<= 10000
<= 50000
<= 100000
<= 500000
> 500000
ADC (mV)
1610
1600
1590
1580
1570
1560
1550
1540
1530
1520
1510
DAC (mV)
1520
1530
1540
1550
1560
1570
1580
1590
1600