Design Advisory: possible timing marginality on QSPI interface for XHRA-2HPA-TQ64-C

Issue description

The Quad SPI interface on the XHRA-2HPA-TQ64-C chips may show a timing marginality under certain PVT conditions. This is because the existing OTP code programmed on these chips makes the quad SPI clock (QSCLK) run continuously regardless of the status of the chip select (CS#) signal, which can cause undefined behaviour if a clock edge occurs too close to a CS# edge. The impact of this issue is that flash operations may fail on chips that are prone to this timing marginality.

Impacted hardware

All XHRA-2HPA-TQ64-C chips with date codes prior to 1610 are susceptible to this issue, unless marked with an additional “R” at the bottom right hand corner of the chip to indicate updated and corrected OTP code has been programmed into the on-chip OTP memory.

For other xCORE-200 chips and hardware from XMOS, a fix has been implemented in the XMOS development tools version 14.2.0 such that QSCLK is not running when CS# is toggled. XMOS recommends that all customers upgrade to the latest version of the tools as published at www.xmos.com/support/tools.

Mitigation

The functionality of the XHRA-2HPA-TQ64-C chips cannot be changed as the on-chip OTP memories are pre-programmed by XMOS. We expect that under most conditions no issues will be observed; however, XMOS will exchange parts free of charge upon request from impacted customers. XMOS recommends that affected parts should not be used in volume production of customers’ products. However, it is okay to use for design prototyping and debugging purpose if the XHRA-2HPA-TQ64-C chips under use do not show any flash operations issue – meaning they don’t suffer from this timing marginality issue.